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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/559,497

12/06/2005

Takehiro Fujii

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EXAMINER

VARNER, MORGAN T

ART UNIT

PAPER NUMBER

2895

MAIL DATE

DELIVERY MODE

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PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b> 10/559,497	<b>Applicant(s)</b> FUJII, TAKEHIRO	
	<b>Examiner</b> MORGAN VARNER	<b>Art Unit</b> 2895	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 06 December 2005.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-4 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-4 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 06 December 2005 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)            | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)   | Paper No(s)/Mail Date. _____                                      |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date <u>6 December 2005</u> .   | 6) <input type="checkbox"/> Other: _____                          |

## DETAILED ACTION

### ***Claim Rejections - 35 USC § 103***

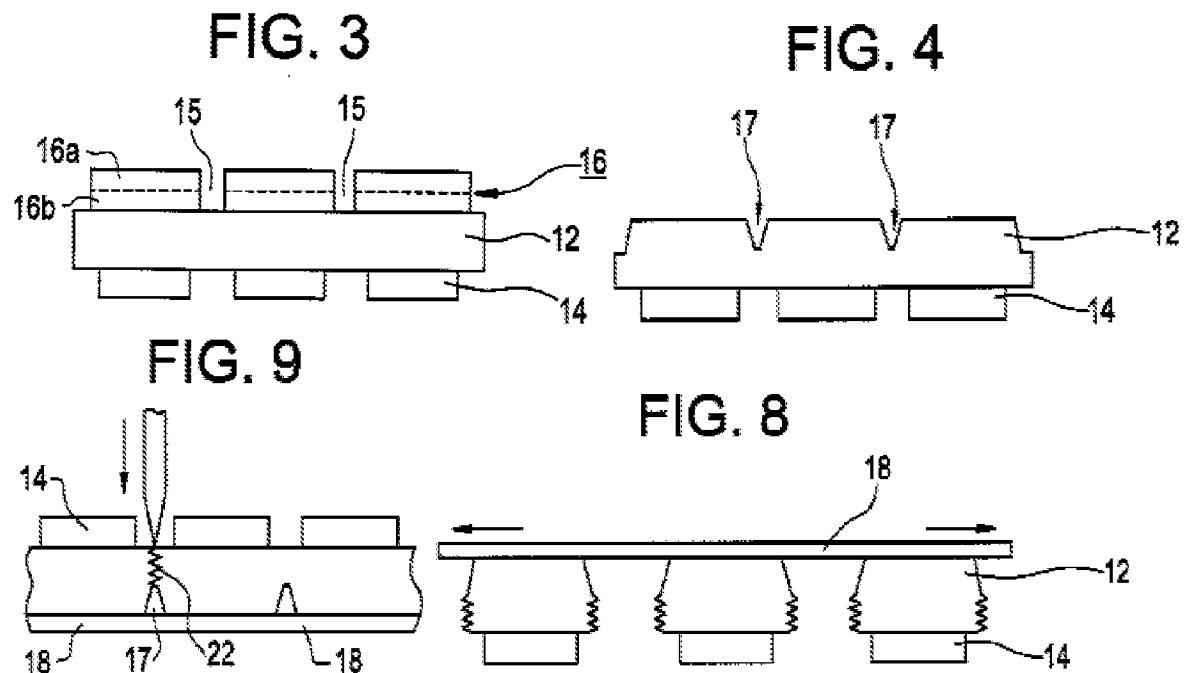
The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yeom et al., US Publication No. 2003/0190770 A1 (filed 9 April 2002) in view of Slater, Jr. et al., US Publication No. 2004/0056260 (provisional application No. 60/411,980 filed 19 September 2002), Slater, Jr. et al., US Publication No. 2002/0123164 A1 (published 5 September 2002), Cobbley et al., US Publication No. 2004/0032013 A1 (filed 15 August 2002).

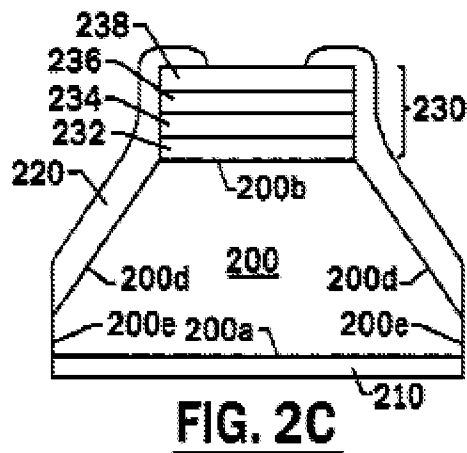


Regarding claim 1, Yeom et al. teaches (from figs. 3, 4, 9 and 8) a method for manufacturing a light-emitting diode element, the method comprising the steps of: preparing an integral LED material plate (12, 14) corresponding to a plurality of LED chips each of which includes an anode and a cathode electrodes for a blue light-emitting layer (electrodes are inherent from "GaN-based LED devices" from p. 3, ¶¶0033-¶¶0034); bonding the LED material plate (12) to an upper surface of an expansion sheet (18) (see "tape" from p. 4, ¶¶0046); dicing the LED material plate (12, 14) into individual LED chips while the LED material plate (12, 14) is bonded to the expansion sheet (18); (from fig. 8) stretching the expansion sheet (18) along a surface so that a spacing between adjacent LED chips (12, 14) is widened;

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*detaching the LED chips from the expansion sheet* (see p. 3 ¶0044 – p. 4, ¶0047; see p. 3, ¶0035-¶0043 for dicing steps before attachment of material plate to expansion sheet).

Yeom et al. does not teach that the LED is a *white LED*, nor does it teach *forming a light-pervious synthetic resin layer containing a fluorescent material so that each of the LED chips is embedded in the synthetic resin layer up to the electrode on an upper surface of the LED chip*. However, Slater, Jr. et al. '260 does teach this limitation.



From fig. 2C, Slater, Jr. et al. '260 teaches a GaN LED structure (see p. 3, ¶0025) with an ohmic contact (230) mounted atop a substrate (200), which in turn is mounted atop a diode region (210). A phosphor-containing layer (220) bound in transparent epoxy (see p. 4, ¶0036 - p. 5, ¶0039) of variable thickness (see ¶0036) is coated on the sidewall of the LED device up to the top-mounted electrode to fluorescently reduce the frequency of the light emitted by the LED. This coating may also be suspended in the packaging and/or encapsulation that is provided with the LED (see p. 2, ¶0010 - ¶0013).

It would have been obvious to one of ordinary skill in the art to modify the invention of Yeom et al. by adding the phosphor/epoxy coating disclosed in Slater, Jr.

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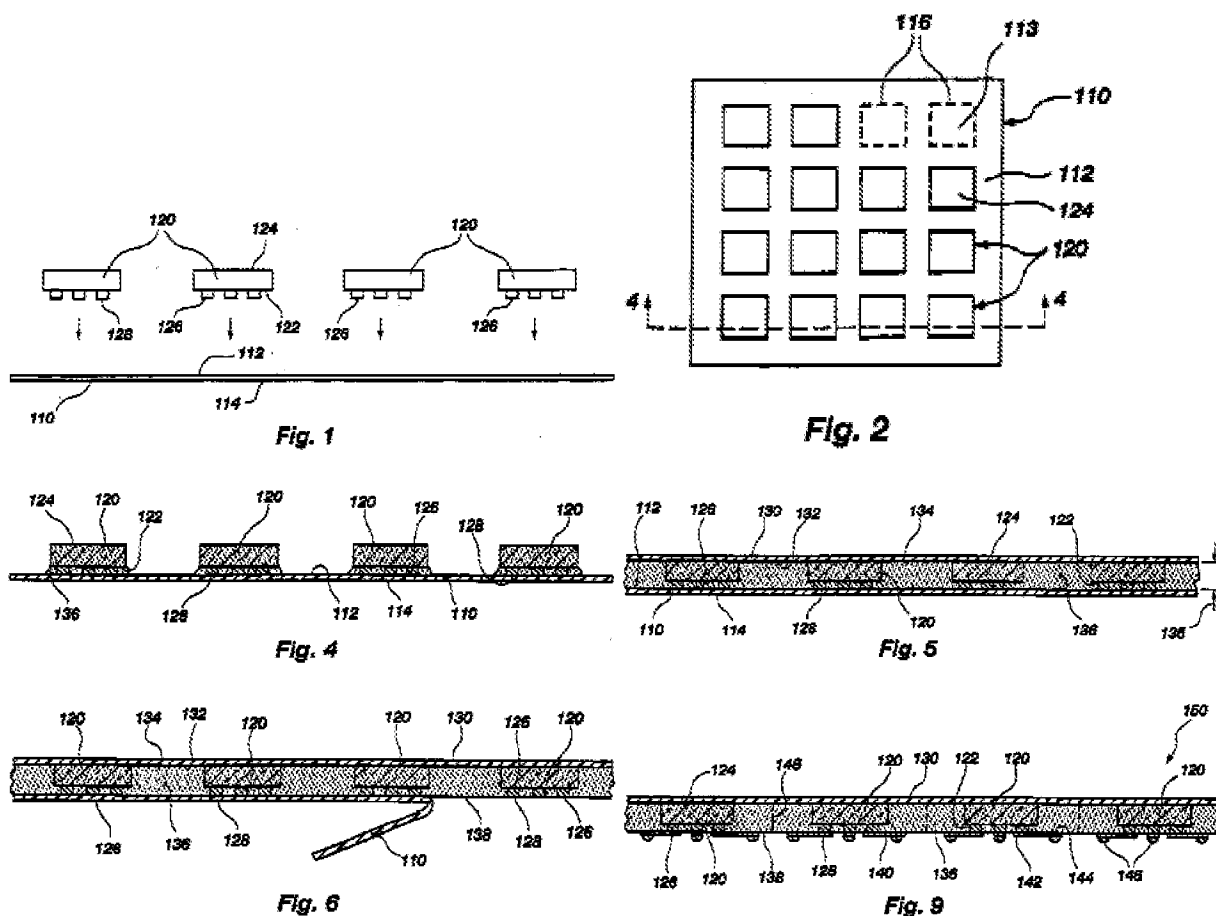
'260, because, as stated in that reference (see p. 2, ¶0013), adding phosphor to blue LED's is a well-known way of producing white light.

Neither Yeom et al. nor Slater, Jr. et al. '260 teaches that *the anode electrode and the cathode electrode are provided respectively at opposite end surfaces of the chip*. However, Slater, Jr. et al. '164, which Slater, Jr. et al. '260 incorporates by reference, does teach this limitation.

From fig. 16, Slater, Jr. et al. '164 teaches a GaN LED package structure including a diode layer (170) with an ohmic contact (150) at its outer-most surface formed opposite a multi-layer ohmic contact structure (1620) relative to a SiC substrate (110) (see p. 9, ¶0085 – p. 10, ¶0092).

It would have been obvious to one of ordinary skill in the art to form the diode layer (210) disclosed in fig. 2C of Slater, Jr., et al. '260 according to Slater, Jr. et al. '164 (i.e. to modify Yeom et al. by forming cathode and anode on opposite end surfaces of the chip) because Slater, Jr. et al. '260 explicitly teaches doing so (see p. 3, ¶0029).

Neither Yeom et al. nor either of the Slater, Jr. et al. references teach that *at least either of the cathode electrode and the anode electrode comes into close contact with the expansion sheet*, nor the step of *dicing the synthetic resin layer to remove portions of the synthetic resin layer between adjacent LED chips by a cutting width which is smaller than the spacing distance between side surfaces of adjacent LED chips*. However, Cobbley et al. does teach this practice.



Cobbley et al. teaches a method for assembling and packaging semiconductor dice wherein singulated dice (120) are mounted via adhesive (113) with conductive leads (126) facing downward in an evenly-spaced distribution on a flexible substrate (110) which may be polyimide tape (see figs. 1,2 and p. 3, ¶0039 – p. 4, ¶0042). Once the dice are secured to the tape, a layer of dielectric filler material (136) which may be epoxy (see fig. 5), is formed on the flexible tape (110) so that it reaches the top surfaces of the dice (see p. 4, ¶0043 – p. 4, ¶0046). As shown in fig. 9, the epoxy layer is later cut along grid lines (148) so as to separate individual devices (see p. 5, ¶0054). As

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shown in fig. 6, the polyimide tape is separated from the bottom surface of each device (see p. 4, ¶0047).

The figures of Yeom et al. only show the expansion sheet being stretched in one dimension, but it would have been obvious to one of ordinary skill in the art at the time of invention to stretch it in two perpendicular directions so as to completely separate individual LED chips on the expansion sheet, because semiconductor processing methods in which individual chips are formed in two-dimensional arrays and subsequently diced along grid lines are very common in the art, and stretching in a second dimension could be effected using the same equipment far more simply than by some other means. Moreover, it might be argued that two-dimensional stretching is not mentioned in Yeom et al. because it is seen as implicit in the teaching that the individual dice should be separated from one another.

It would also have been obvious to one of ordinary skill in the art at the time of invention to combine the process of Yeom et al. as modified according to the two Slater et al. references with the invention of Cobbley et al. by beginning Cobbley's process at the step shown in figs. 2 and 3 after Yeom's dicing process and before the LED's are removed from the tape, and suspending phosphor within the epoxy encapsulant as explicitly suggested in Slater, Jr. et al. '260 in p. 2, ¶0013. If encapsulation is performed while the LED's are still on the original tape surface, no additional steps will be required to re-calibrate or re-align the work pieces for later processes such as the cutting step.

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Regarding claim 2, Yeom et al. in view of Slater, Jr. et al. '260 and '164, and further in view of Cobbley et al. teach *the method for manufacturing a white light-emitting diode element according to claim 1*. Yeom et al. (see figs. 3-4 and p. 3, ¶¶0035-¶0043) Slater, Jr. et al. '260 teaches that *dicing of the LED material plate into individual LED chips comprises forming an inclined surface (17) at a side surface of each of the LED chips, the inclined surface being inclined from one electrode film toward the other electrode film*. Slater, Jr. et al. '260 also teaches this limitation (see p. 4, ¶0034).

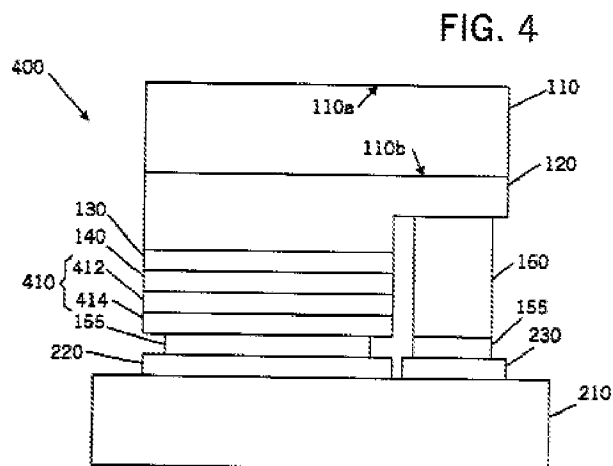
Regarding claim 3, Yeom et al. in view of Slater, Jr. et al. '260 and '164, and further in view of Cobbley et al. teach *the method for manufacturing a white light-emitting diode element according to claim 1*, and from fig. 2C and p. 5, ¶0040 Slater, Jr. et al. '260 teaches that *each of the LED chips includes a light reflective layer (234) on an upper side of the light-emitting layer (210)*.

Regarding claim 4, Yeom et al. teaches a method of manufacturing a light-emitting diode element, the method comprising the steps of:  
preparing an integral LED material plate corresponding to a plurality of LED chips each of which includes an anode and a cathode electrodes for a blue light-emitting layer (see "GaN-based LED devices" from p. 3, ¶¶0033-¶0034);  
*bonding the LED material plate (12, 14) to an upper surface of an expansion sheet (18)* (see "tape from p. 4, ¶0046);

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licing the LED material plate (12, 14) into individual LED chips while the LED material plate is bonded to the expansion sheet (18); stretching the expansion sheet (18) in two directions which are perpendicular to each other along a surface (as explained in the rejection to claim 1) so that a spacing between adjacent LED chips is widened (see p. 3 ¶0044 – p. 4, ¶0047).

Slater, Jr. et al. '164 further teaches (from fig. 4) that *the anode electrode and the cathode electrode (220 and 230) are provided at an end surface of the LED chip* (see p. 6, ¶0056).



Cobbley et al. teaches (figs. 1 and 2 and p. 3, ¶0039 – p. 4, ¶0042) that *the cathode electrode and the anode electrode (126) come into close contact with the expansion sheet (110).*

As explained in the rejection of claim 1 above, Cobbley et al. and Slater, Jr. et al. '260 together teach *forming a light-pervious synthetic resin layer containing a fluorescent material on the upper surface of the expansion sheet so that each of the*

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*LED chips is embedded in the synthetic resin layer at least up to a side surface (see Cobbley et al. p. 4, ¶¶0043 - ¶¶0046; see Slater, Jr. et al. '260 in p. 2, ¶¶0013).*

Cobbley et al. further teaches *dicing the synthetic resin layer to remove portions of the synthetic resin layer between adjacent LED chips by a cutting width which is smaller than the spacing distance between side surfaces of adjacent LED chips (see fig. 9 and p. 4, ¶¶0054).*

Cobbley et al. (from fig. 6 and p. 4, ¶¶0047) and Yeom et al. (see p. 4, ¶¶0046) both further teach detaching the LED chips from the expansion sheet.

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MORGAN VARNER whose telephone number is (571)270-7397. The examiner can normally be reached on Monday-Friday 07:30 - 17:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Drew N. Richards can be reached on (571) 272-1736. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/MORGAN VARNER/  
Examiner, Art Unit 2895  
24 March 2009

/N. Drew Richards/  
Supervisory Patent Examiner, Art Unit 2895